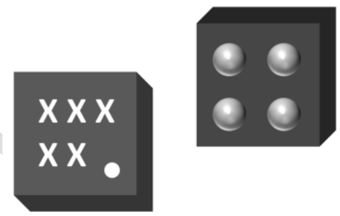
3-Axis Single Chip Magnetic Sensor

QMC6308

The QMC6308 is a three-axis magnetic sensor, which integrates magnetic sensors and signal condition ASIC into one silicon chip. This wafer level chip scale package (WLCSP) is targeted for applications such as e-compass, map rotation, gaming and personal navigation in mobile and wearable devices.



The QMC6308 is based on state-of-the-art, high resolution, magneto-resistive technology. Along with the custom-designed 16-bit ADC ASIC, it offers the advantages of low noise, high accuracy, low power consumption, offset cancellation and temperature compensations. QMC6308 enables 1° to 2° compass heading accuracy. The I²C serial bus allows for easy interface.

The QMC6308 is in a 0.8x0.8x0.5mm^3 surface mount 4-pin WLCSP package.

FEATURES	BENEFIT
3-Axis Magneto-Resistive Sensors in a 0.8x0.8x0.5 mm^3 WLCSP, Guaranteed to Operate Over an Extended Temperature Range of -40 °C to +85 °C.	Small Size for Highly Integrated Products. Signals Have Been Digitized and Calibrated.
16 Bit ADC With Low Noise AMR Sensors Achieves 2 milli-Gauss Field Resolution	Enables 1° To 2° Degree Compass Heading Accuracy, Allows for Pedestrian Navigation and LBS Applications
Wide Magnetic Field Range (±30 Gauss)	Maximizes Sensor's Full Dynamic Range and Resolution
Temperature Compensated Data Output	Automatically Maintains Sensor's Sensitivity Under Wide Operating Temperature Range
I²C Interface with Standard and Fast Modes	High-Speed Interfaces for Fast Data Communications. Maximum 1.5KHz Data Output Rate
Built-In Self-Test	Enables Low-Cost Functionality Test After Assembly in Production
Wide Range Operation Voltage (1.65V to 1.95V) and Low Power Consumption (15µA)	Compatible with Battery Powered Applications
Lead Free Package Construction	RoHS Compliance
Software and Algorithm Support Available	Compassing Heading, Hard Iron, Soft Iron, and Auto Calibration Libraries Available

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1 INTERNAL SCHEMATIC DIAGRAM

1.1 Internal Schematic Diagram

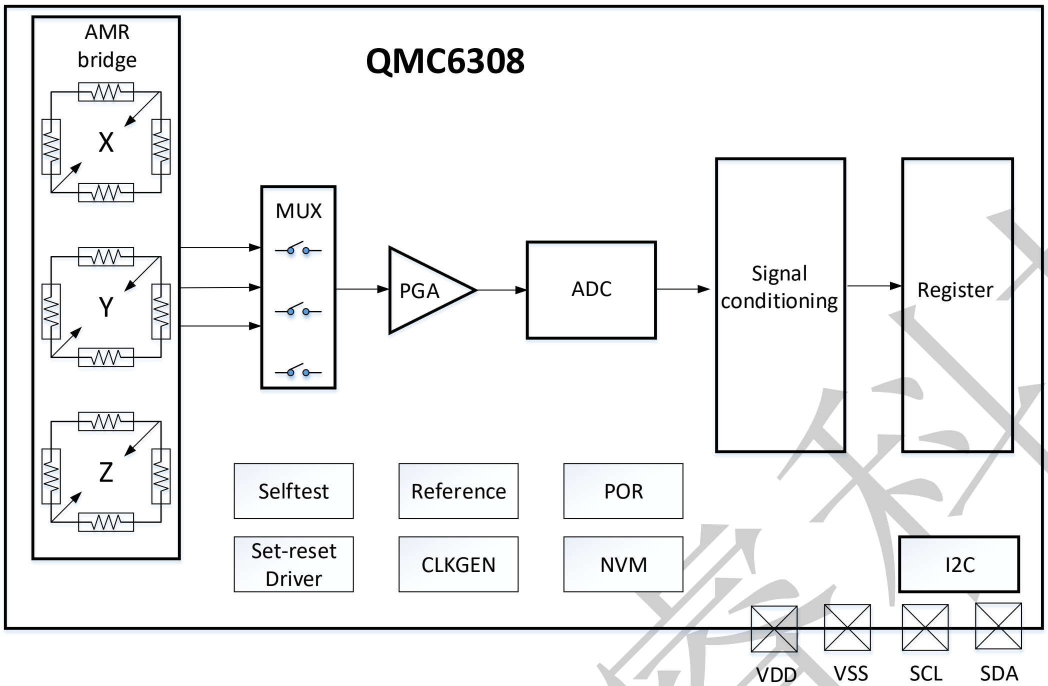


Figure 1. Block Diagram

Table 1. Block Function

Block	Function
AMR bridge	3-axis magnetic sensor
MUX	Multiplexer for sensor channels
PGA	Programmable gain amplifier for sensor signals
ADC	Analog-to-Digital converter
Signal conditioning	Digital blocks for magnetic signal calibration and compensations
I^2C	Interface logic data I/O
NVM	Non-volatile memory
Register	Internal register
Selftest	Internal driver to generate self-test stimulus
Set-reset Driver	Internal driver to initialize magnetic sensor
Reference	Voltage/current reference for internal biasing
CLKGEN.	Internal oscillator for internal operation
POR	Power on reset

2 SPECIFICATIONS AND I/O CHARACTERISTICS

2.1 Product Specifications

Table 2. Specifications (Tested and specified at 25°C, VDD=1.8V, except stated otherwise.)

Parameter	Conditions		Min	Typ	Max	Unit
Supply Voltage	VDD		1.65		1.95	V
Suspend Mode Current[3]	Total Current on VDD			2	3	µA
Normal Mode Current [1]	Low power and high power mode	ODR=10Hz		15/58		uA
		ODR=50Hz		65/290		
		ODR=100Hz		130/580		
		ODR=200Hz		260/1160		
Continuous Mode Current[3]	Maximum ODR: 1500Hz			2200	2800	uA
Sensor Field Range	Full Scale		-30		30	Gauss
Sensitivity [2,3]	±30G		-5		5	%
	Field Range = ±30G			1000		LSB/G
	Field Range = ±12G			2500		LSB/G
	Field Range = ±8G			3750		LSB/G
	Field Range = ±2G			15000		LSB/G
Linearity[3]	Field Range = ±30G Happlied= ±15G			0.5	0.7	%FS
Hysteresis[3]	3 sweeps across ±30G			0.03	0.06	%FS
Offset				±10		mG
Sensitivity Tempco[3]	Ta = -40°C~85°C				±0.05	%/°C
Digital Resolution	Field Range = ±30G			1.0		mGauss
Field Resolution[3]	Standard deviation			3	6	mGauss
X-Y-Z Orthogonality[3]	Sensitivity Directions			90±1	90±3	Degree
Operating Temperature			-40		85	°C
ESD	HBM		4000			V
	CDM		1000			

Note [1]: The Normal Mode Current differs at different OSR1 setting. The value of low power mode is measured at OSR1=1 setting， and the value of high power mode is measured at OSR1=8.
Note [2]: Sensitivity is calibrated at zero field; it is slightly decreased at high fields.
Note [3]: Based on 3lots characterization results at continuous mode

2.2 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings (Tested at 25°C except stated otherwise.)

Parameter	MIN.	MAX.	Units
VDD	-0.3	2.0	V
Storage Temperature	-40	125	°C
Exposed to Magnetic Field (all directions)		50000	Gauss
Reflow Classification	MSL 1, 260 °C Peak Temperature		

2.3 I/O Characteristics

Table 4. I/O Characteristics（VDDIO=1.8V）

Symbol	Parameter(Units)	Minimum	Typical	Maximum
V_{IH}	High Level Input Voltage(V)	0.7*VDDIO		
V_{IL}	Low Level Input Voltage(V)			0.3*VDDIO
V_{HYS}	Hysteresis of Schmitt Trigger Input(V)	0.1		
I_{IL}	Input Leakage, ALL Inputs(uA)	-10		10
V_{OH}	High Level output Voltage(V)	0.8*VDDIO		
V_{OL}	Low Level output Voltage(V)			0.2*VDDIO

3 PACKAGE PIN CONFIGURATIONS

3.1 Package 3-D View

Arrow indicates direction of magnetic field that generates a positive output reading in normal measurement configuration.

< QMC6308 >

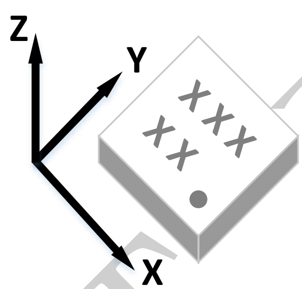


Figure 2. Package 3-D View

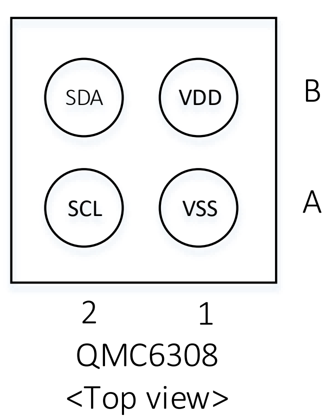


Figure 3. Package Top View

Table 5. Pin Configurations

PIN No.	PIN NAME	I/O	TYPE	Function
A1	VSS		Power	Ground
A2	SCL	I	CMOS	I2C clock
B1	VDD		Power	Supply Voltage
B2	SDA	I/O	CMOS	I2C data

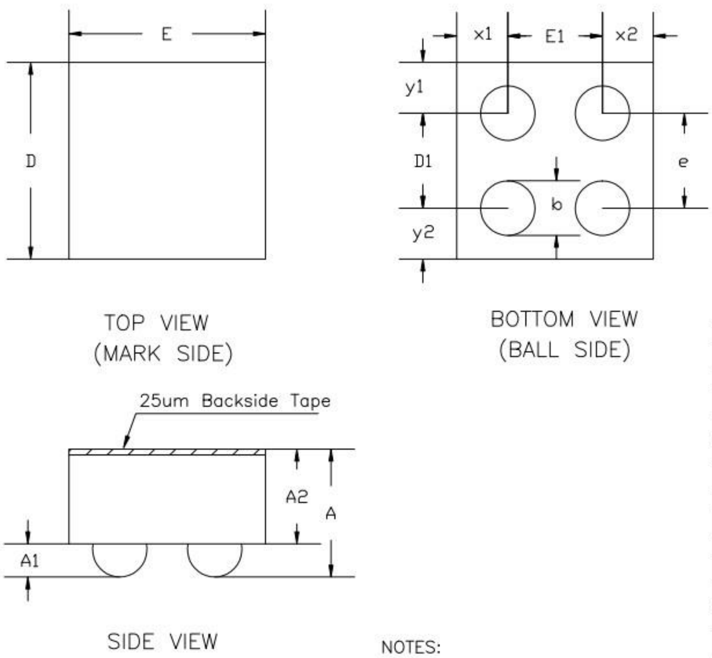
3.2 Package Outlines

3.2.1 Package Type

WLCSP

3.2.2 Package Size:

0.8mm (Length)*0.8mm (Width)*0.5mm (Height)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.510	0.540	0.570
A1	0.110	0.140	0.170
A2	0.375	0.400	0.425
D	0.810	0.830	0.850
E	0.810	0.830	0.850
D1		0.400BSC	
E1		0.400BSC	
e		0.400BSC	
b	0.200	0.230	0.260
x1		0.215REF	
x2		0.215REF	
y1		0.215REF	
y2		0.215REF	

Figure 4. Package Size

3.2.3 Marking:

Tracking code: $X_1X_2X_3X_4X_5$

X_1= Supplier code
$X_2X_3X_4X_5$= Package Lot
●= Pin1 Identifier

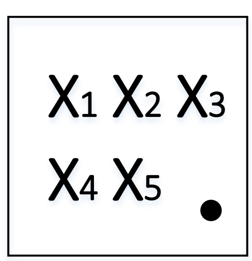


Figure 5. Chip Marking

4 EXTERNAL CONNECTION

4.1 Recommended External Connection

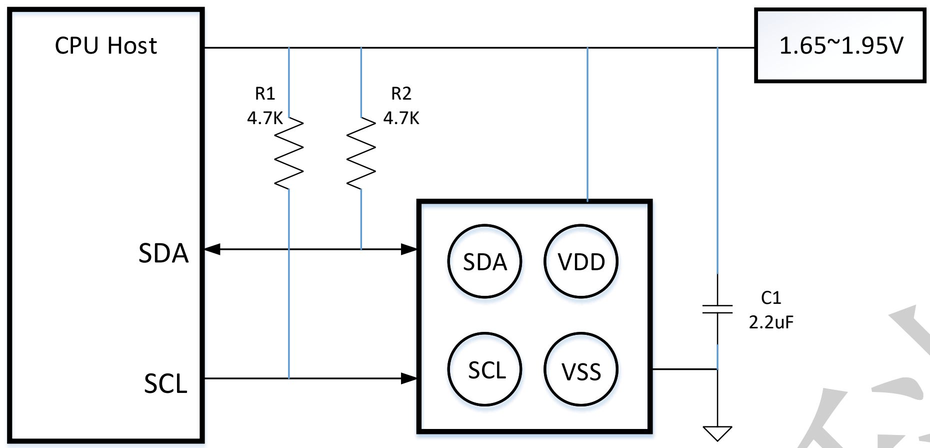


Figure 6. External Connection

Note: R1/R2 selection guide: 2.7Kohm for a short I2C bus length (less than 10 cm), and 4.7Kohm for a bus length less than 5 cm.

4.2 Mounting Considerations

The following is the recommend printed circuit board (PCB) footprint for the QMC6308. Due to the fine pitch of the pads, the footprint should be properly centered in the PCB.

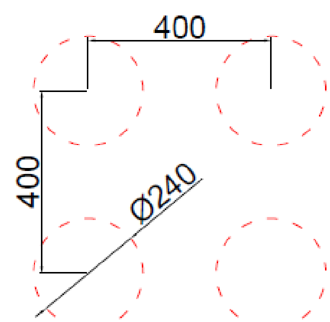


Figure 7. QMC6308 PCB footprint

4.3 Layout Considerations

Besides keeping all components that may contain ferrous materials (nickel, etc.) away from the sensor on both sides of the PCB, it is also recommended that there is no conducting copper line under/near the sensor in any of the PCB layers.

4.3.1 Solder Paste

A 4-mil stencil and 100% paste coverage is recommended for the electrical contact pads.

4.3.2 Reflow Assembly

This device is classified as MSL 1 with 260°C peak reflow temperature. Reference IPC/JEDEC standard J-STD-033 for additional information.

No special reflow profile is required for QMC6308, which is compatible with lead eutectic and lead-free solder paste reflow profiles. QST recommends adopting solder paste manufacturer's guidelines. Hand soldering is not recommended.

4.3.3 External Capacitors

The external capacitors C1 should be ceramic type with low ESR characteristics. The exact ESR value is not critical, but values less than 200 milli-ohms are recommended. Reservoir capacitor C1 is nominally 2.2 µF in capacitance. Low ESR characteristics may not be in many small SMT ceramic capacitors (0402), so be prepared to up-size the capacitors (0201) to gain low ESR characteristics.

5 BASIC DEVICE OPERATION

5.1 Anisotropic Magneto-Resistive Sensors

The QMC6308 magneto-resistive sensor circuit consists of tri-axial sensors and application specific support circuits to measure magnetic fields. With a DC power supply is applied to the sensor two terminals, the sensor converts any incident magnetic field in the sensitive axis directions to a differential voltage output.

The device has an offset cancellation function to eliminate sensor and ASIC offsets. It also applies a self-aligned magnetic field to restore magnetic state before each measurement to ensure high accuracy. Because of these features, the QMC6308 doesn't need to calibrate every time in most of application situations. It may need to be calibrated once in a new system or a system changes a new battery.

5.2 Power Management

There are only one power supply pins to the device. VDD provides power for all the internal analog and digital functional blocks and I/O.

When the device is powered on, all registers are reset by POR (Power-On-Reset), then the device transits to the suspend mode and waits for further commands.

Table 6 provides references for two power states.

Table 6: Power States

Power State	VDD	Power State description
1	0V	Device Off, No Power Consumption
2	1.65V~1.95V	Device On, Enters Suspend Mode after POR, waiting for further commands

5.3 Power On/Off Time

After the device is powered on, some time periods are required for the device fully functional. The external power supply requires a time period for voltage to ramp up (PSUP), it is typically 50 milli-second. However, it isn't controlled by the device. The Power-On-Reset time period (PORT) includes time to reset all the logics, load values in NVM to proper registers, enter the standby mode and get ready for analogy measurements. The power on/off time related to the device is in Table 7.

Table 7. Time Required for Power On/Off

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
POR Completion Time	PORT	Time Period After VDD at Operating Voltage to Ready for I²C Command			250	uS
Power off Voltage	SDV	Voltage that Device Considered to be Power Down.			0.2	V
Power on Interval	PINT	Time Period Required for Voltage Lower Than SDV to Enable Next POR	100			uS

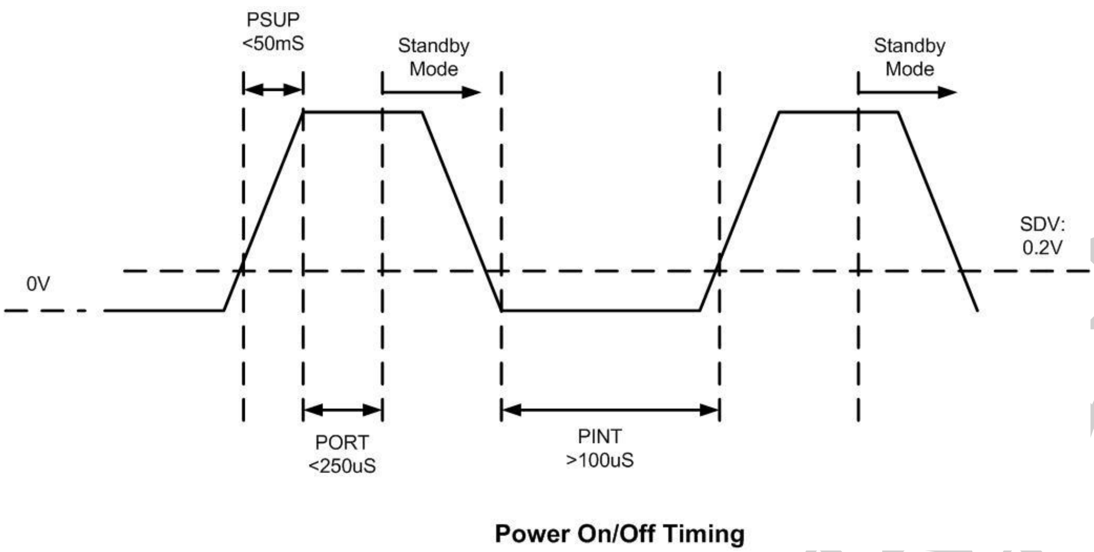


Figure 8. Power On/Off Timing

5.4 Communication Bus Interface I²C and Its Addresses

This device will be connected to a serial interface bus as a slave device under the control of a master device, such as the processor. Control of this device is carried out via I²C.

This device is compliant with I²C Bus Specification. As an I²C compatible device, this device has a 7-bit serial address and supports I²C protocols. This device supports standard and fast speed modes, 100kHz and 400kHz, respectively. External pull-up resistors are required to support all these modes.

There are only one I²C address available. The default value is 2CH.

5.5 Internal Clock

The device has an internal clock for internal digital logic functions and timing management. This clock is not available to external usage.

5.6 Temperature Compensation

The Device has built-in Temperature compensation function. The compensated magnetic sensor data is placed in the Output Data Registers automatically.

6 MODES OF OPERATION

6.1 Modes Transition

The device has three different modes, controlled by register (0x0A), mode bits Mode<1:0>. The main purpose of these modes is for power management. The modes can be transited from one to another, as shown below, through I²C commands of changing mode bits. The default mode is Suspend Mode.

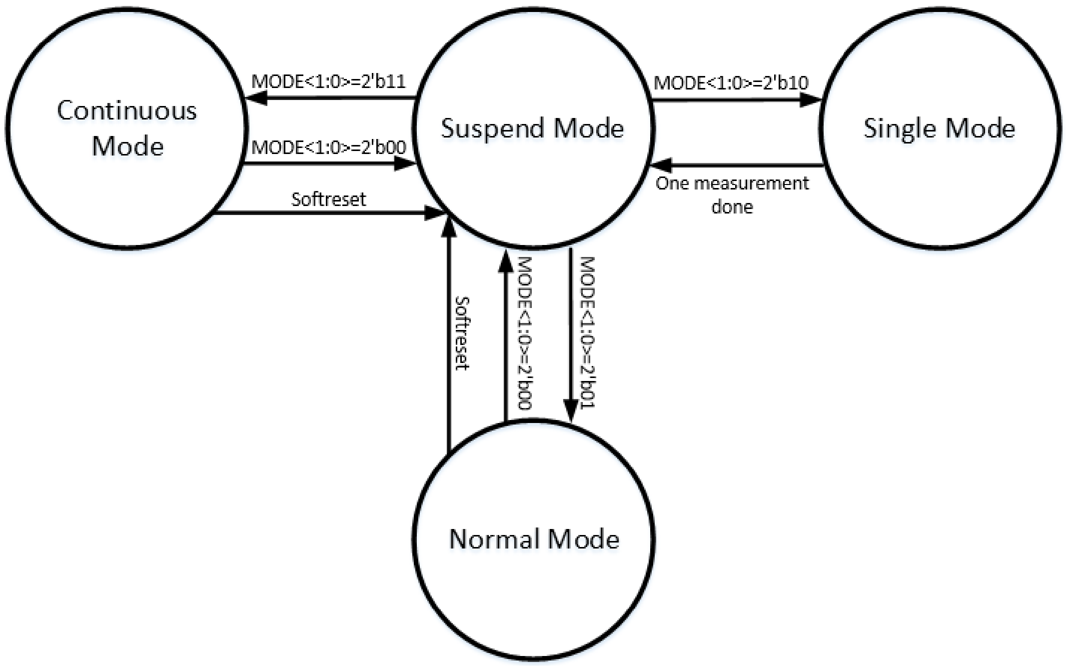


Figure 9. Modes Transition

6.2 Description of Modes

6.2.1 Normal Mode

During the Normal mode (MODE bits= 2'b01), the magnetic sensor continuously makes measurements and places measured data in data output registers. The field range register is controlled by RNG<1:0> in register 0BH and data output rate is controlled by ODR<1:0> in register 0AH. They should be set up properly for your applications in the normal mode.

6.2.2 Single Mode

During the Single Mode (MODE bits=2'b10), the whole chip runs only once and enter in the suspend mode after 1 measurement is finished.

6.2.3 Continuous Mode

During the Continuous Mode (MODE bits=2'b11), the whole chip runs all the time without sleep time, so the maximum ODR can be got at this mode. The self-test function can only be enabled in Continuous Mode and enters in Suspend Mode after the data is updated.

6.2.4 Suspend Mode

Suspend mode is the default magnetometer state upon POR and soft reset. Only few function blocks are activated in this mode which keeps power consumption as low as possible. In this state, register values are hold on by a lower power LDO, I2C interface is active and all register read and write are allowed. There is no magnetometer measurement in this Mode.

7 APPLICATION EXAMPLES

7.1 Normal Mode Setup Example

- ✧ Write Register 0BH by 0x00 (Define Set/Reset mode, with Set/Reset On, Field Range 30Guass)
- ✧ Write Register 0AH by 0xCD (set normal mode, set ODR=200Hz)

7.2 Continuous Mode Setup Example

- ✧ Write Register 0BH by 0x00 (Define Set/Reset mode, with Set/Reset On, Field Range 30Guass)
- ✧ Write Register 0AH by 0xC3 (set continuous mode)

7.3 Self-test Example

- ✧ Write Register 0AH by 0x03 (set continuous mode)
- ✧ Check status register 09H[0] ,"1" means ready
- ✧ Read data Register 01H ~ 06H, recording as datax1/datay1/dataz1
- ✧ Write Register 0BH by 0x40(enter self-test function)
- ✧ Waiting 5 millisecond until measurement ends
- ✧ Read data Register 01H ~ 06H, recording as datax2/datay2/dataz2
- ✧ Calculate the delta DeltaX=(datax1-datax2), DeltaY=(datay1-datay2), DeltaZ=(dataz1-dataz2)
- ✧ Self-test Judgment: If the delta value of each axis is in the range of following table, the chip is working properly.

	DeltaX	DeltaY	DeltaZ
Criteria（Unit:LSB）	800~1200	800~1200	120~1200

7.4 Suspend Mode Example

- ✧ Write Register 0AH by 0x00

7.5 Measurement Example

- ✧ Check status register 09H[0] ,"1" means ready
- ✧ Read data register 01H ~ 06H

7.6 Soft Reset Example

- ✧ Write Register 0BH by 0x80

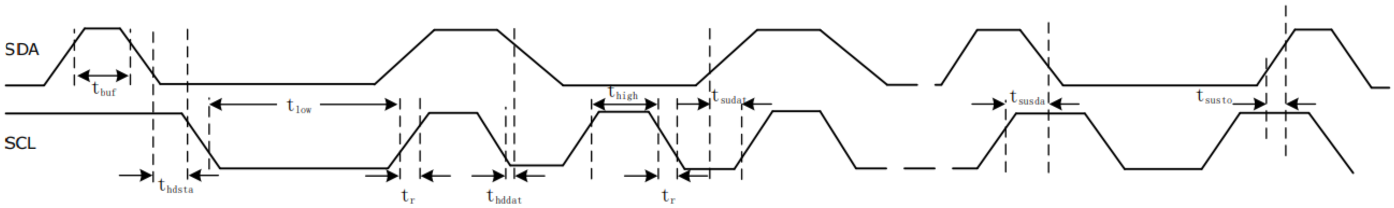
8 I²C COMMUNICATION PROTOCOL

8.1 I²C Timings

Below table and graph describe the I²C communication protocol times

Table 8. I²C Timings

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
SCL Clock		f_{scl}		0		400	kHz
SCL Low Period		t_{low}		1			μS
SCL High Period		t_{high}		0.6			μS
SDA Setup Time		t_{sudat}		0.1			μS
SDA Hold Time		t_{hddat}		0			μS
Start Hold Time		t_{hdsta}		0.6			μS
Start Setup Time		t_{susta}		0.6			μS
Stop Setup Time		t_{susto}		0.6			μS
New Transmission Time		t_{buf}		1.3			μS
Rise Time		t_r				0.3	μS
Fall Time		t_f				0.3	μS



I²C Timing Diagram

Figure 10. I²C Timing Diagram

8.2 I²C R/W Operation

8.2.1 Abbreviation

Table 9. Abbreviation

SACK	Acknowledged by slave
MACK	Acknowledged by master
NACK	Not acknowledged by master
RW	Read/Write

8.2.2 Start/Stop/Ack

START: Data transmission begins with a high to transition on SDA while SCL is held high. Once I²C transmission starts, the bus is considered busy.
STOP: STOP condition is a low to high transition on SDA line while SCL is held high.
ACK: Each byte of data transferred must be acknowledged. The transmitter must release the SDA line during the acknowledge pulse while the receiver must then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.
NACK: If the receiver doesn't pull down the SDA line during the high period of the acknowledge clock cycle, it's recognized as NACK by the transmitter.

8.2.3 I²C Write

I²C write sequence begins with start condition generated by master followed by 7 bits slave address and a write bit (R/W=0). The slave sends an acknowledge bit (ACK=0) and releases the bus. The master sends the one-byte register address. The slave again acknowledges the transmission and waits for 8 bits data which shall be written to the specified register address. After the slave acknowledges the data byte, the master generates a stop signal and terminates the writing protocol.

Table 10. I²C Write

START	Slave Address							RW	SACK	Register Address (0x0A)								SACK	Data (0x01)								SACK	STOP
	0	1	0	1	1	0	0	0		0	0	0	0	1	0	1	0		0	0	0	0	0	0	0	1		

8.2.4 I²C Read

I²C read sequence consists of a one-byte I²C write phase followed by the I²C read phase. A start condition must be generated between two phases. The I²C write phase addresses the slave and sends the register address to be read. After slave acknowledges the transmission, the master generates again a start condition and sends the slave address together with a read bit (R/W=1). Then master releases the bus and waits for the data bytes to be read out from slave. After each data byte, the master has to generate an acknowledge bit (ACK = 0) to enable further data transfer. A NACK from the master stops the data being transferred from the slave. The slave releases the bus so that the master can generate a STOP condition and terminate the transmission.

Table 11. I²C Read

S	Slave Address	RW	S	Register Address (0x00)	S

	0	1	0	1	1	0	0	0		0	0	0	0	0	0	0	0		
START	Slave Address							R W	SACK	Data (0x00)								NACK	STOP
	0	1	0	1	1	0	0	1		0	0	0	0	0	0	0	0		

9 REGISTERS

9.1 Register Map

The table below provides a list of the 8-bit registers embedded in the device and their respective function and addresses.

Chip ID is located at the address 00H, the default value is 80H. It can be used to recognize device.

Table 12. Register Map

Addr.	7	6	5	4	3	2	1	0	Access	Value after por or soft reset
00H	Chip ID								Read only	80H
01H	Data Output X LSB Register XOUT[7:0]								Read only	00H
02H	Data Output X MSB Register XOUT[15:8]								Read only	00H
03H	Data Output Y LSB Register YOUT[7:0]								Read only	00H
04H	Data Output Y MSB Register YOUT[15:8]								Read only	00H
05H	Data Output Z LSB Register ZOUT[7:0]								Read only	00H
06H	Data Output Z MSB Register ZOUT[15:8]								Read only	00H
09H	-	-	-	NVM_LD	NVM_RDY	-	OVFL	DRDY	Read only	18H
0AH	OSR2<1:0>		OSR1<1:0>		ODR<1:0>		MODE<1:0>		Read/Write	00H
0BH	SOFT_RST	SELF_TEST	RFU		RNG<1:0>		SET/RESET MODE<1:0>		Read/Write	00H/80H*
0DH	-	SR_CTRL	-	-	-	-	-	-	Read/Write	00H
29H	-	-	-	-	-	SIGNZ	SIGNY	SIGNX	Read/Write	00H

*For 0BH, the value is 00H after POR, and 80H after soft reset, because the SOFT_RST bit is not auto-cleared after setting high.

9.2 Register Definition

9.2.1 Output Data Register

Registers 01H ~ 06H store the measurement data from each axis magnetic sensor in each working mode. In the normal mode, the output data is refreshed periodically based on the data update rate ODR setup in control registers 0AH. The data stays the same, regardless of reading status through I²C, until new data replaces them. Each axis has 16-bit data width in 2's complement, i.e., MSB of 02H/04H/06H indicates the sign of each axis. The output data of each channel saturates at -32768 and 32767.

Table 13. Output Data Register

Addr.	7	6	5	4	3	2	1	0
01H	Data Output X LSB Register XOUT[7:0]							
02H	Data Output X MSB Register XOUT[15:8]							
03H	Data Output Y LSB Register YOUT[7:0]							
04H	Data Output Y MSB Register YOUT[15:8]							
05H	Data Output Z LSB Register ZOUT[7:0]							
06H	Data Output Z MSB Register ZOUT[15:8]							

9.2.2 Status Register

There is one status register located in address 09H.
Register 09H has two bits indicating for status flags, the rest are reserved for factory use. The status registers are read only bits.

Table 14. Status Register 1

Addr.	7	6	5	4	3	2	1	0
09H			NVM_ LD	NVM_ RDY			OVFL	DRDY

DRDY bit denotes the status of data, which is set when all three-axis data is ready and loaded to the output data registers in each mode. It is reset to “0” by reading the status register through I^2C commands
DRDY: “0”: no new data, “1”: new data is ready

OVFL bit is set high when either axis code output exceeds the range of [-30000,30000] LSB and reset to “0” after the status register is read.
OVFL: “0”: no data overflow occurs, “1”: data overflow occurs

NVM_RDY denotes the status of built-in Non-volatile Memory.
NVM_RDY: “0”: NVM not ready for access, “1”: NVM ready for access

NVM_LD denotes the status of data loading from built-in Non-volatile Memory
NVM_LD: “0”: data loading from NVM not finished, “1”: data loading from NVM finished

9.2.3 Control Registers

Two 8-bits registers are used to control the device configurations.
Control register 1 is located in address 0AH, it sets the operational modes (MODE) and over sampling rate (OSR).
Control register 2 is located in address 0BH. It controls soft reset, self-test and set/reset mode.

Two bits of MODE registers can transfer mode of operations in the device, the four modes are Suspend Mode, Normal mode, Single Mode and Continuous Mode. The default mode after Power-On-Reset (POR) is Suspend Mode. Suspend Mode should be added in the middle of mode shifting between Continuous Mode、Single Mode and Normal Mode.

The Output data rate is controlled by ODR registers. Four data update frequencies can be selected: 10Hz, 50Hz, 100Hz or 200Hz.

Over sample Rate (OSR1) registers are used to control bandwidth of an internal digital filter. Larger OSR value leads to smaller filter bandwidth, less in-band noise and higher power consumption. It could be used to reach a good balance between noise and power. Four over sample ratio can be selected, 8,4,2 or 1.
Another filter is added for better noise performance; the depth can be adjusted through OSR2.

Table 15. Control Register 1

Addr	7	6	5	4	3	2	1	0
0AH	OSR2<1:0>		OSR1<1:0>		ODR<1:0>		MODE<1:0>	

Reg.	Definition	00	01	10	11
Mode	Mode Control	Suspend	Normal Mode	Single	Continuous Mode
ODR	Output Data Rate	10Hz	50Hz	100Hz	200Hz
OSR1	Over sample Ratio1	8	4	2	1
OSR2	Down sampling rate	1	2	4	8

Set/Reset Mode can be control by the register SET/RESET MODE. There are 3 modes for selection：SET AND RESET ON， SET ONLY ON and SET AND RESET OFF. In SET ONLY ON or SET AND RESET OFF mode, the offset is not renewed during measuring.

Field ranges of the magnetic sensor can be selected through the register RNG. The full-scale range is determined by the application environments. The lowest field range has the highest sensitivity, therefore, higher resolution.

Self-test function is added for verification of the signal-chain. When the function is enable through the bit SELF—_TEST, a inner-built current is generated and an additional signal is added to the sensor, generating a difference in the 3 axis value. User should record the value before and after the self-test and compare with threshold value.

Soft reset can be done by setting the register SOFT_RST High. Soft reset can be invoked at any time of any mode. After setting High, the SOFT_RST bit will not be auto-cleared. So after the soft reset command 0BH=80, another command 0BH=00 is always needed.

Table 16. Control Register 2

Addr.	7	6	5	4	3	2	1	0
0BH	SOFT_RST	SELF_TEST	-	-	RNG<1:0>		SET/RESET MODE<1:0>	

Reg.	Definition	00	01	10	11
SET/RESET MODE	Set and reset mode ctrl	Set and reset on	Set only on	Set and reset off	Set and reset off
RNG	Full Range	30Guass	12Guass	8Guass	2Guass
SELF_TEST	Self_test	1: self_test enable, auto clear after the data is updated			
SOFT_RST	Soft reset	1：Soft reset, restore default value of all registers，0: no reset			

There are 2 more registers used for better set-reset performance and signal sign configuration.
SR_CTRL control bit is located at address 0x0D<6>. When this bit is set high, the interior set reset coil will generate a larger current, which results better set-reset performance.

SR_PW<2:0> is located at address 0x29<6:4>. It controls the pulse width of set-reset.

PT bit is located at address 0x29<3>. Every time the set-reset pulse comes, there might be a relatively large voltage turbulence on the power supply, so it is meaningful to reserve a short period of time for power stabilizing. PT is used to control this duration.

There are 3 bits for controlling the sign of 3 axis magnetic digital output, naming SIGNZ SIGNY and SINGX. They are located at the address 0x29<2:0>.

Table 17. Control Register 3

Addr	7	6	5	4	3	2	1	0
0DH		SR_ CTRL						

Reg.	Definition	0	1
SR_CTRL	Set-Reset control	Normal set-reset current level	Increased set-reset current level

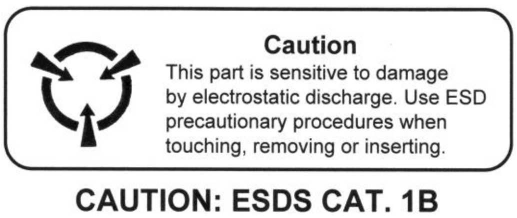
Table 18. Control Register 4

Addr	7	6	5	4	3	2	1	0
29H	-	-	-	-	-	SIGNZ	SIGNY	SIGNX

Reg.	Definition	0	1
SIGNZ	Sign of Z axis	Positive sign	Negative sign
SIGNY	Sign of Y axis		
SIGNX	Sign of X axis		

ORDERING INFORMATION

Ordering Number	Operating Temperature	Package	Packaging
QMC6308-TR	-40°C ~ 85°C	WLCSP	Tape and Reel: 5k pieces/reel



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For more information on QST's Magnetic Sensors contact us at 86-21-69517300.

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U.S. Patents 4,441,072, 4,533,872, 4,569,742, 4,681,812, 4,847,584 and 6,529,114 apply to the technology described.

China Patents 201210563667.3, 201210563956.3, 201210563952.5, 201210563687.0, 201310403912.9, 201410027189.3, 201410027240.0, 201410027085.2 and 201410085278.3 apply to the technology described.